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| EXAMINER | |
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| MCMAHON, DANIEL F | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/577,288 | GOESSEL ET AL. | |
| | Examiner | Art Unit | |
| | DANIEL F. MCMAHON | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *30-53 and 55-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-53 and 55-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the applicant's amendment dated 12/11/2008.

Claims 1 – 29, 54, and 61 – 63 are cancelled.

Claims 30, 32 – 35, 37 – 48, 51 – 53, and 55 – 60 have been amended.

Claims 30 – 53 and 55 – 60 are pending.

### *Response to Amendment*

1. The objection to claims 34, 39, 41 – 44, 46 – 48, 54 – 58 for the language "one of" is withdrawn in light of amendment to the claims.

2. The objection to claims 39 as being a substantial duplicate of claim 37 is withdrawn in light of amendment to the claims.

3. The objection to claims 45 is withdrawn in light of amendment to the claims.

4. The objection to claims 54 is withdrawn in light of the cancellation of claim 54.

Regarding rejections under 35 U.S.C. 112, second paragraph:

5. The rejection of claims 32 – 34, and 37 – 47, for the use of "coded", "coding", and "codes" is withdrawn in light of the amendment to the claims.

6. The rejection of claims 32, 41 – 44, and 47 for improper antecedent basis is withdrawn in light of the amendment to the claims.

7. The rejection of claim 51, 52, and 56 for indefiniteness due to ambiguous language is withdrawn in light of the amendment to the claims.

8. The rejection of claim 53 for improper antecedent basis is maintained. Applicant states the claim has been amended to provide proper antecedent basis for the limitations “k” and “t”. Examiner is unable to determine how claim 53 was amended to provide proper antecedent basis for the limitation “k”.

9. The rejection of claim 63 for improper antecedent basis is withdrawn in light of the cancellation of the claim.

Regarding rejections under 35 U.S.C. 101:

10. The rejection of claim 53 for failure to recite a tangible element is withdrawn in light of the amendment to the claims.

11. The rejection of claim 54 is withdrawn in light of the cancellation of the claim.

12. The rejection of claims 59 and 60 is maintained. The claims fail to recite a tangible element for the product and are therefor non-statutory subject matter.

13. The rejection of claims 61 - 63 are withdrawn in light of the cancellation of the claims.

***Response to Arguments***

14. Applicant's arguments, regarding Hasegawa, filed December 11, 2008, with respect to the rejection of claim 30 under 35 U.S.C. 102, have been fully considered but are not persuasive.

Applicant argues Hasegawa does not disclose "a common input line for receiving a data stream". Applicant asserts that the collective compression unit 16 and not the scan chain unit 2 receives the signals Dpa to Dpn. However, Hasegawa clearly discloses "The scan chain compression unit receives the test results Dpa to Dpn in parallel" (paragraph 0066, page 5, lines 9 – 10), which is the same input as collective compression unit 16 (paragraph 0065, page 4, lines 31 – 35).

Applicant additionally argues "wherein the first linear automaton circuit and the second linear automation circuit are configured such that a first signature can be calculated from each data word and a second signature can be calculated from each data word." Applicant relies on Hasegawa paragraph 0065 to state that scan chain compression unit 2 compresses only one output of dpa to dpn and does not calculate with dpa to dpn. Examiner is unclear what text the applicant relies upon for this assertion. Hasegawa clearly discloses scan chain compression unit 2 compresses dpa to dpn (paragraph 0066, page 5, lines 10 – 17).

15. Applicant's arguments, regarding Hasegawa and Meaney, filed December 11, 2008, with respect to the rejection of claims 31 – 52 and 56 – 58 under 35 U.S.C. 103, have been fully considered but are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the use of an XOR logic gate is well known in the art for the purpose of comparison. Specifically, Meaney teaches XOR comparison logic to ensure parallel operation of integrated circuits (Meaney: abstract).

Applicant's argument regarding claim 30 was not persuasive, therefore the rejection of dependant claims 31 – 52 and 56 – 58 is maintained.

16. In view of applicant's arguments examiner maintains the previous prior art rejections.

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The following claims are rejected under 35 U.S.C. 112, second paragraph:

2. Claim 53 recites "k". There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 59 and 60 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. “A computer program product” is non-statutory subject matter. Applicant has failed to recite a physical media for the computer program. Therefor the claim is not directed at a useful process, machine, manufacture, or composition of matter, or improvement thereof. MPEP 2106.01

### *Prior Art Rejections*

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 30 is rejected under 35 U.S.C. 102(a) as being anticipated by Hasegawa et al. U.S. Publication 2004/0246337 (herein Hasegawa).

6. Regarding claim 30, Hasegawa discloses an evaluation circuit (figure 4) comprising: a first linear automation circuit (figure 4, element 16); a second linear automation circuit connected in parallel with the first linear automation circuit (figure 4, element 2), each having a set of states, which have a common input line for receiving a data stream (paragraph 0066), Tn comprising n successive data words y(1), … y(n), each having a width of k bits, wherein the first linear automaton circuit and the second linear automation circuit are configured such that a first signature can be calculated from each data word and a second signature can be calculated from each data word (paragraph 0066); a first logic combination gate (figure 4, element 4) and a second logic combination gate (figure 4, element 6) that compare the first signature and the second

signature, respectively, with a predeterminable good signature and an output comparison value (paragraph 65, lines 35 – 38; paragraph 66, lines 32 – 35).

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 31, 32, 35 – 37, 39, 41 - 45, 48 - 52, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. U.S. Publication 2004/0246337 (herein Hasegawa), in view of Meaney, U.S. Patent 6,055,660 (herein Meaney).

9. Regarding claim 31, Hasegawa teaches the limitations of the parent claim, claim 30. Hasegawa does not explicitly teach: a first logic combination gate and the second combination logic gate are exclusive-OR gates having first inputs, respectively, connected to the outputs of the associated first and second linear automaton circuit and to whose second inputs good signatures can be applied.

Meaney teaches: a first logic combination gate and the second combination logic gate are exclusive-OR gates having first inputs, respectively, connected to the outputs of the associated first and second linear automaton circuit and to whose second inputs good signatures can be applied (figure 2, element 13, element 22).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, a first and second logic combination gate, with the teaching of Meaney, a first and second logic combination gate as an XOR gate. The use of XOR logic gates for comparison is well known in the art (column 4, line 13, element 22) and the combination would yield a predictable result.

10. Regarding claim 32, Hasegawa teaches the limitations of the parent claim, claim 30. Hasegawa does not explicitly teach: upstream of the first linear automaton circuit is a first coder, that encodes a data word having the data word length of k bits into an encoded data word $u^1(i)$, $u^1(i)$=Cod1 having the word width of K1 bits, for i = 1, ..., n, and where Cod1 represents the encoding function of the first coder.

Meaney teaches: upstream of the first linear automaton circuit is a first coder, that encodes a data word having the data word length of k bits into an encoded data word $u^1(i)$, $u^1(i)$=Cod1 having the word width of K1 bits, for i = 1, ..., n, and where Cod1 represents the encoding function of the first coder (figure 2, element 21).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: a first coder upstream of the first linear automation circuit for the purpose of detection of errors introduced independent of the design under test. Data coders are a well known technique in the art for detecting errors in data. One of ordinary skill in the art, at the time of the invention, would have recognized the application of the known technique would have yielded predicable results.

11. Regarding claim 35, Hasegawa teaches: an evaluation circuit for detecting and/or locating faulty data words in a data stream Tn (abstract) comprising: a first linear automaton circuit and a second linear automaton circuit connected in parallel (figure 4, element 2, element 16), each having a set of states, wherein the first linear automaton circuit and the second linear automaton circuit have a common input line for receiving a data stream Tn comprising n successive data words y(1), ..., y(n) each having a width of k bits, (figure 4); a first logic combination gates arranged downstream of the first linear automaton circuit and also a second logic combination gates arranged downstream of the second linear automaton circuit, (figure 4, element 4, element 6); the logic combination gates are designed such that the signature respectively calculated by the linear automaton circuit can be compared with a predeterminable good signature and a comparison value can be output (paragraph 65, lines 35 – 38; paragraph 66, lines 32 – 35); and the first linear automaton circuit and the second linear automaton circuit are designed such that a first signature and a second signature, respectively, can be calculated of each data word (paragraph 0066, page 5, lines 15 – 17).

Hasegawa does not explicitly teach: the first linear automaton circuit can be described by the following equation $z(t + 1) = Az(t)$ XOR $y(t)$; the second linear automaton circuit can be described by the following equation $z(t+ 1) = Bz(t)$ XOR $y(t)$; and where A and B represent the state matrices of the linear automaton circuits, where the state matrices A and B can be inverted, and where the dimension L of the state vectors is $\geq k$.

Meaney teaches: the first linear automaton circuit can be described by the following equation z(t + 1) = Az(t) XOR y(t) (column 3, lines 23 – 33, table 2); the second linear automaton circuit can be described by the following equation z(t+ 1) = Bz(t) XOR y(t) (column 3, lines 23 – 33, table 2); and where A and B represent the state matrices of the linear automaton circuits, where the state matrices A and B can be inverted, and where the dimension L of the state vectors is ≥ k (column 3, lines 23 – 33; table 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa: a first linear automaton circuit and a second linear automaton circuit connected in parallel, and a first logic combination gates arranged downstream of the first linear automaton circuit and a second logic combination gates arranged downstream of the second linear automaton circuit, with the teaching of Meaney: a linear automaton circuit can be described by the following equation z(t + 1) = Az(t) XOR y(t) and A can be inverted, for the purpose of creating a test vector signature for comparison purposes (abstract, lines 4 – 7). A first linear automaton circuit, also known as a Multiple-input Shift Register (MISR) with the function z(t + 1) = Az(t) XOR y(t) is a well known design choice in the art, and the use of the well known design choice would yield predictable results.

12. Regarding claim 36, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: the logic combination gates are present as exclusive-OR gates whose first inputs are respectively connected to the

outputs of the associated linear automaton circuit and to whose second inputs good signatures can be applied.

Meaney teaches: the logic combination gates are present as exclusive-OR gates whose first inputs are respectively connected to the outputs of the associated linear automaton circuit and to whose second inputs good signatures can be applied. (figure 2, element 13, element 22)

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, a first and second logic combination gate, with the teaching of Meaney, a first and second logic combination gate as an XOR gate. The use of XOR logic gates for comparison is well known in the art (column 4, line 13, element 22) and the combination would yield a predictable result.

13. Regarding claim 37, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: arranged upstream of the first linear automaton circuit is a first coder, that encodes the data word y(i) having the data word length of k bits into an encoded data word ul(i), ul(i)=Cod1 having the word width of K1 bits, for i=l, ..., n, and where Cod1 represents the encoding function of the first coder.

Meaney teaches: arranged upstream of the first linear automaton circuit is a first coder, that encodes the data word y(i) having the data word length of k bits into a coded data word ul(i), ul(i)=Cod1 having the word width of K1 bits, for i=l, ..., n, and where Cod1 represents the encoding function of the first coder (figure 2, element 21).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: a first coder upstream of the first linear automation circuit for the purpose of detection of errors introduced independent of the design under test. Data encoders are a well known technique in the art for detecting errors in data. One of ordinary skill in the art, at the time of the invention, would have recognized the application of the known technique would have yielded predicable results.

14. Regarding claim 39, Hasegawa and Meaney teach the limitations of the parent claim, claim 37. Hasegawa does not explicitly teach: arranged upstream of the second linear automaton circuit is a second coder, which encodes the data word y(i) having the data word length of k bits into an encoded data word u2(i), u2(i)=Cod2(y(i)) having the word width of K2 bits, for i=1, ..., n, and where Cod2 represents the encoding function of the second coder.

Meaney teaches: arranged upstream of the second linear automaton circuit is a second coder (figure 2, element 21'), which encodes the data word y(i) having the data word length of k bits into an encoded data word u2(i), u2(i)=Cod2(y(i)) having the word width of K2 bits, for i=1, ..., n, and where Cod2 represents the encoding function of the second coder (figure 2, element 21').

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: a second coder upstream of the second linear automation

circuit for the purpose of detection of errors introduced independent of the design under test. Data encoders are a well known technique in the art for detecting errors in data. One of ordinary skill in the art, at the time of the invention, would have recognized the application of the known technique would have yielded predicable results.

15. Regarding claim 41, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the word width K1 of the data words u1(i) encoded by the first coder is equal to the word width K2 of the data words u2(i) encoded by the second coder.

Meaney teaches: the word width K1 of the data words u1(i) encoded by the first coder is equal to the word width K2 of the data words u2(i) encoded by the second coder (figure 2, element 23, element 23').

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: the first coder and second coder having the same data output width for the purpose of providing symmetric data protection for the first and second path. It is a well known design technique to replicate logic units to minimize design and test of logic elements. One of ordinary skill in the art at the time of the invention would recognize that applying the known technique would yield predictable results.

16. Regarding claim 42, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the first coder matching the second coder with regard to its construction and its function.

Meaney teaches: the first coder matching the second coder with regard to its construction and its function. (figure 2, element 23, element 23')

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: the first coder and second coder having the same construction and function. It is a well known design technique to replicate logic units to minimize design and test of logic elements. One of ordinary skill in the art at the time of the invention would recognize that applying the known technique would yield predictable results.

17. Regarding claim 43, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the word width K1 of the data words $u^1(i)$ encoded by the first coder and the word width K2 of the data words $u^2(i)$ encoded by the second coder are in each case equal to the word width k of the data words y(1), ..., y(n) of the data stream Tn.

Meaney teaches: the word width K1 of the data words $u^1(i)$ encoded by the first coder and the word width K2 of the data words $u^2(i)$ encoded by the second coder are in each case equal to the word width k of the data words y(1), ..., y(n) of the data stream

Tn. (figure 2, element 25, element 22, element 23, element 25', element 22', element 23')

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: the first coder and second coder having the same data width of $u^1(i)$ and $u^2(i)$ as y(i). It is a well known design technique to replicate logic units to minimize design and test of logic elements. One of ordinary skill in the art at the time of the invention would recognize that applying the known technique would yield predictable results.

18. Regarding claim 44, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the encoding functions Cod1 and Cod2 of the first coder and of the second coder are designed as follows:

$Cod1(y_1(i), y_2(i), ..., y_k(i)) = Pl(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$

$Cod2(y_l(i), y_2(i), ..., y_k(i)) = P2(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$

For i, 1, ..., n where the number of zeros situated at the end of $P1(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$ is equal to (K1-k), where the number at the end of $P2(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$ is equal to (K2-k), and where P 1 represents an arbitrary permutation of the K1 components of $(y_1(i), y_2(i), ..., y_k(i), 0, ...,0)$ and P2 represents an arbitrary permutation of the K2 components of $(y_1(i), y_2(i), ..., y_k(i), 0, ...,0)$ (figure 2, element 23, element 24, element 23', element 24').

Meaney teaches: the encoding functions Cod1 and Cod2 of the first coder and of the second coder are designed as follows:

$Cod1(y_1(i), y_2(i), ..., y_k(i)) = Pl(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$

$Cod2(y_l(i), y_2(i), ..., y_k(i)) = P2(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$

For i, 1, ..., n where the number of zeros situated at the end of $P1(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$ is equal to (K1-k), where the number at the end of $P2(y_l(i), y_2(i), ..., y_k(i), 0, ..., 0)$ is equal to (K2-k), and where P 1 represents an arbitrary permutation of the K1 components of $(y_1(i), y_2(i), ..., y_k(i), 0, ...,0)$ and P2 represents an arbitrary permutation of the K2 components of $(y_1(i), y_2(i), ..., y_k(i), 0, ...,0)$ (figure 2, element 23, element 24, element 23', element 24').

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Meaney, zero padding of code words. Zero padding of code words in a known technique in the art, and the combination would yield predictable results.

19. Regarding claim 45, Hasegawa and Meaney teach the limitations of the parent claim, claim 37. Hasegawa does not explicitly teach: the coding functions Cod1 and Cod2 of the first coder and of the second coder are designed as follows:

$Cod1(y_1(i), y_2(i), ..., y_k(i)) = P1(y_1(i), y_2(i), ..., y_k(i), b_1{}^1..., b_{K1}{}^1{}_k)$

$Cod2(y_l(i), y_2(i), ..., y_k(i)) = P2(y_l(i), y_2(i), ..., y_k(i), b_1{}^2..., b_{K1}{}^2{}_K)$

and where P1 and P2 represent arbitrary permutations.

Meaney teaches: the coding functions Cod1 and Cod2 of the first coder and of the second coder are designed as follows:

$Cod1(y_1(i), y_2(i), ..., y_k(i)) = P1(y_1(i), y_2(i), ..., y_k(i), b_1^1..., b_{K1}{}^1{}_k)$

$Cod2(y_l(i), y_2(i), ..., y_k(i)) = P2(y_l(i), y_2(i), ..., y_k(i), b_1^2..., b_{K1}{}^2{}_K)$

and where P1 and P2 represent arbitrary permutations (figure 2, element 23, element 24, element 23', element 24').

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Meaney, padding of code words with $b_1^n..., b_{K1}{}^n{}_k$. Padding of code words in a known technique in the art, and the combination would yield predictable results.

20. Regarding claim 48, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: the state matrix A of the first linear automaton circuit and the state matrix B of the second linear automaton circuit are related to one another as follows: $B = A^n$ where $n \neq 1$.

Meaney teaches: the state matrix A of the first linear automaton circuit and the state matrix B of the second linear automaton circuit are related to one another as follows: $B = A^n$ where $n \neq 1$ (table 2)

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Meaney, matrix $B = A^n$ where $n \neq 1$. Inverted matrices

are a well known design choice in MISR design is well known in the art, and combination would yield predictable results.

21. Regarding claim 49, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: the state matrix B of the second linear automaton circuit is equal to the inverted state matrix $A^{-1}$ of the first linear automaton circuit.

Meaney teaches: the state matrix B of the second linear automaton circuit is equal to the inverted state matrix $A^{-1}$ of the first linear automaton circuit (table 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Meaney, matrix $B = A^{-1}$. Inverted matrices are a well known design choice in MISR design is well known in the art, and combination would yield predictable results.

22. Regarding claim 50, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: the first linear automaton circuit is designed as a linear feedback shift register and the second linear automaton circuit is designed as an inverse linear feedback shift register, both linear automaton circuits having a parallel input.

Meaney teaches: the first linear automaton circuit is designed as a linear feedback shift register and the second linear automaton circuit is designed as an

inverse linear feedback shift register, both linear automaton circuits having a parallel input (table 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Meaney, the linear automaton circuits as linear feedback shift registers. Implementation of a linear automaton circuit as a linear feedback shift register is a well known design choice in the art and the combination would yield a predictable result.

23. Regarding claim 51, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa additionally teaches: the first linear automaton circuit is designed as a linear feedback, multi-input shift register or the second linear automaton circuit is designed as a linear feedback, multi-input shift register. (figure 4, element 16, element 2)

24. Regarding claim 52, Hasegawa and Meaney teach the limitations of the parent claim, claim 52. Hasegawa additionally teaches: the multi- input shift registers have a primitive feedback polynomial of maximum length (paragraph 0081).

25. Regarding claim 55, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa additionally teaches: the evaluation circuit is monolithically integrated on an integrated circuit (abstract).

26. Claims 33, 34, 38, 40, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Meaney, in view of Applicant Admitted Prior Art (herein AAPA).

27. Regarding claim 33, Hasegawa and Meaney teach the limitations of the parent claim, claim 32. Hasegawa does not explicitly teach: the encoding function of the first coder as:

Cod1 (y'(i)) = u1(i) XOR f1(e(i)), or

Cod1 (y'(i)) = Cod1(y(i) XOR e(i)) = Cod1 (y(i) XOR $f_1$(e(i))

where a function $f_1$ by $f_1$ (0) = 0, exists for y'(i) = y(i) XOR e(i), and where a function $f_1^{-1}$ where $f_1^{-1}$ ($f_1$(e)) = e, exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn.

AAPA teaches: the encoding function of the first coder as:

Cod1 (y'(i)) = u1(i) XOR f1(e(i)), or

Cod1 (y'(i)) = Cod1(y(i) XOR e(i)) = Cod1 (y(i) XOR $f_1$(e(i))

where a function $f_1$ by $f_1$ (0) = 0, exists for y'(i) = y(i) XOR e(i), and where a function $f_1^{-1}$ where $f_1^{-1}$ ($f_1$(e)) = e, exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a first coder upstream of a first linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

28. Regarding claim 34, Hasegawa teaches the limitations of the parent claim, claim 30. Hasegawa does not explicitly teach: arranged upstream of the second linear automaton circuit is a second coder, which encodes the data word y(i) having the data word length of k bits into an encoded data word u2(i), u2(i)=Cod2(y(i)) having the word width of K.2 bits, for i=l, ..., n, and where Cod2 represents the encoding function of the second coder.

Meaney teaches: arranged upstream of the second linear automaton circuit is a second coder (Meaney: figure 2, element 21'),

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa, an evaluation circuit, as cited above, with the teaching of Meaney: a second coder upstream of the second linear automation circuit for the purpose of detection of errors introduced independent of the design under test. Data encoders are a well known technique in the art for detecting errors in data. One of ordinary skill in the art, at the time of the invention, would have recognized the application of the known technique would have yielded predicable results.

Meaney does not explicitly teach: which encodes the data word y(i) having the data word length of k bits into an encoded data word u2(i), u2(i)=Cod2(y(i)) having the word width of K.2 bits, for i=l, ..., n, and where Cod2 represents the encoding function of the second coder.

AAPA teaches: which encodes the data word y(i) having the data word length of k bits into an encoded data word u2(i), u2(i)=Cod2(y(i)) having the word width of K.2 bits, for i=l, ..., n, and where Cod2 represents the encoding function of the second coder (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a second coder upstream of the second linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

29. Regarding claim 38, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: the following holds true for the encoding function of the first coder:

Codl (y'(i)) = ul(i) (D $f_1$(e(i)), or

Cod1 (y'(i)) = Cod1 (y(i) XOR e(i)) = Cod1 (y(i) XOR $f_1$(e(i))

where a function $f_1$ by $f_1(0) = 0$ exists for $y'(i) = y(i)$ XOR $e(i)$, and where a function $f_1^{-1}$ where $f_1^{-1}(f_1(e)) = e$ exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn,

AAPA teaches: the following holds true for the encoding function of the first coder:

Codl $(y'(i)) = ul(i)$ (D $f_1(e(i))$, or

Cod1 $(y'(i))$ = Cod1 $(y(i)$ XOR $e(i))$ = Cod1 $(y(i)$ XOR $f_1(e(i))$

where a function $f_1$ by $f_1(0) = 0$ exists for $y'(i) = y(i)$ XOR $e(i)$, and where a function $f_1^{-1}$ where $f_1^{-1}(f_1(e)) = e$ exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a first coder upstream of a first linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

30. Regarding claim 40, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the following holds true for the encoding function of the second coder:

Cod2(y'(i)) = u2(i) ~ f2(e(i)), or

Cod2(y'(i)) = Cod2(y(i) • e(i)) = Cod2(y(i)) • f2(e(i))

where a function $f_2^{-1}$ where $f_2^{-1}(f_2(e)) = e$ exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn.

AAPA teaches: the following holds true for the encoding function of the second coder:

Cod2(y'(i)) = u2(i) ~ f2(e(i)), or

Cod2(y'(i)) = Cod2(y(i) • e(i)) = Cod2(y(i)) • f2(e(i))

where a function $f_2^{-1}$ where $f_2^{-1}(f_2(e)) = e$ exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream Tn (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a first coder upstream of a first linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

31. Regarding claim 46, Hasegawa and Meaney teach the limitations of the parent claim, claim 37. Hasegawa does not explicitly teach: the encoding function Cod1 of the first coder is designed such that it realizes a linear block code, f1=Cod1.

AAPA teaches: the encoding function Cod1 of the first coder is designed such that it realizes a linear block code, f1=Cod1 (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a first coder upstream of a first linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

32. Regarding claim 47, Hasegawa and Meaney teach the limitations of the parent claim, claim 39. Hasegawa does not explicitly teach: the encoding function Cod2 of the second coder is designed such that it realizes a linear block code, f2=Cod2.

AAPA teaches: the encoding function Cod2 of the second coder is designed such that it realizes a linear block code, f2=Cod2 (page 6, lines 14 – 18).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, with a first coder upstream of a first linear automation circuit, with the teaching of AAPA:, as cited above. Linear block codes, as defined above, are well known technique in the art for error detection correction. One of ordinary skill, at the time of the invention, would have recognized that application of the known technique would yield predictable results.

33. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Meaney, in view of Eldridge et al., U.S. Publication 2001/0052786 (herein Eldridge).

34. Regarding claim 56, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: A load board for receiving at least one needle card for testing integrated circuits or having at least one test socket for testing integrated circuits or for connecting a handler to a tester of integrated circuits, the load board having an evaluation circuit.

Eldridge teaches: A load board for receiving at least one needle card for testing integrated circuits (paragraph 0075).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Eldridge, a load board for receiving a needle card. A load board from receiving a needle card is well known in the art and one of ordinary skill in the art, at the time of invention, would recognize the combination would yield predictable results.

35. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Meaney, in view of Beer, U.S. Publication 2002/0153918 (herein Beer).

36. Regarding claim 57, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: a needle card for testing integrated circuits.

Beer teaches: a needle card for testing integrated circuits (abstract).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Beer, a needle card. A needle card is well known in the art and one of ordinary skill in the art, at the time of invention, would recognize the combination would yield predictable results.

37. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa, Meaney, and Eldridge, in view of Davis et al., U.S. Patent 6,194,910 (herein Davis).

38. Regarding claim 58, Hasegawa and Meaney teach the limitations of the parent claim, claim 35. Hasegawa does not explicitly teach: a tester for testing integrated circuits having the following features: the tester is provided with a plurality of instruments for generating signals or data streams and with a plurality of measuring sensors, in particular for currents and voltages; the tester has a load board which is provided for receiving at least one needle card for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits and/or which is equipped with at least one test socket for testing integrated circuits.

Eldridge teaches: the tester has a load board which is provided for receiving at least one needle card for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits and/or which is equipped with at least one test socket for testing integrated circuits (paragraph 0075).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Eldridge, a load board for receiving a needle card. A load board from receiving a needle card is well known in the art and one of ordinary skill in the art, at the time of invention, would recognize the combination would yield predictable results.

Eldridge does not explicitly teach: the tester is provided with a plurality of instruments for generating signals or data streams and with a plurality of measuring sensors, in particular for currents and voltages.

Davis teaches: the tester is provided with a plurality of instruments for generating signals or data streams and with a plurality of measuring sensors, in particular for currents and voltages (abstract).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Hasegawa and Meaney, an evaluation circuit, as cited above, with the teaching of Davis, a tester for measurement of voltage and current. A tester for measurement of voltage and current is well known in the art and one of ordinary skill in the art, at the time of invention, would recognize the combination would yield predictable results.

***Allowable Subject Matter***

39. Claim 53 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

40. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to discloses or teach:

undergoing transition to the state $z^2(n+1)= S_2(L2, y(1) ...., y(i-1), y(i), y(i+l) .... , y(n))$ if no error can be detected in the case of the data words u2(1), ..., u2(i-1), u2(i), u2(i), ..., u2(n),

undergoing transition to the state $z^2(n+1)= S_2(L2, y(1), ..., y(i-1), y(i), y'(i), y(i+l), ..., y(n))$ if an error is present at least in the case of the i-th position of the coded data words u2(1) ..... u2(i-1), u2'(i), u2(i) .... , u2(n),

the signature of an error-free data stream Tn being designated by S(L2, y(1), ..., y(i-l), y(i), y(i+l), ..., y(n)) and the signature of a faulty data stream Tn being designated by S(L2, y(l), ..., y(i-1), y'(i), ..., y(n)),

determining the signature differences $\Delta S1$ and $\Delta S2$ by means of exclusive-OR logic combinations of the signatures S1 and S2 with ascertained good signatures, in each case according to the following specifications:

$\Delta S1= S(L1, y(1), ..., y(i-1), y(i), y(i+l), ..., y(n))$

XOR S(L1, y(1), ..., y(i-1), y'(i), y(i+l)..., y(n))

$\Delta S2= S(L2, y(1), ..., y(i-1), y(i), y(i+l), ..., y(n))$

XOR S(L2, y(1), ..., y(i-1), y'(i), y(i-~l), ..., y(n))

determining a unique solution for the position i of the faulty bit in the faulty data word by solving the equation $f_1^{-1}(A^{i-n} \Delta S1) = f_2^{-1}(B^{i-n} \Delta S2)$

and if no unique solution results for $1 \leq i \leq n$, outputting a notification by means of an output medium that two or more errors are present in the data stream T, under consideration,

determining a unique solution for the counter e(i) of the faulty data word y'(i) in the data stream Tn by solving the equation

$e(i) = f_1^{-1}(A^{i-n} \Delta S1)$

outputting the position i of the faulty bit in the faulty data word and also the error e(i) of the faulty data word y'(i) in the data stream Tn by means of an output medium.

## *Conclusion*

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dworski et al U.S. Patent 7,391,349

Hasegawa et al. U.S. Publication 2004/0246337

Cote et al. U.S. Publication 2004/0003329

Mattes U.S. Patent 5,224,107

Lim et al. U.S. Patent 6,483,373

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Dfm
02/27/2009